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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,486	01/10/2002	Franco Motika	POU920000199US1	6710

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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,486	MOTIKA ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/26/2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the applicant's amendment dated 10/26/2004.

Claims 4-6 and 8 were amended by the applicant.

New Claims 9-14 were added by the applicant.

Claims 1-14 are now pending.

Response to Amendment

As per Objections to the Specification and Drawings:

1. In view of the applicant's changes to the Abstract, Specification, and Drawings, the examiner withdraws all objections, and approves the changes.

As per Rejections under 35 USC 112 2nd Paragraph:

2. In view of the amendment to Claim 4, the examiner withdraws the rejection of Claim 4 under 35 USC 112 2nd paragraph.

3. In view of the amendment to Claim 8, the examiner maintains the rejection of Claim 8 under 35 USC 112 2nd paragraph as having insufficient antecedent basis for the amended limitation in the claim. The phrase, "the stuck-at fault memory condition" lacks antecedent basis.

Response to Arguments

4. Applicant's arguments filed 10/26/2004, regarding Claims 1-8, have been fully considered but they are not persuasive. In the argument, the applicant has stated that the IBM reference has failed to teach, "triggering a change in state to

introduce data into a inaccessible latches in a stuck-at fault LSSD chain", and , "triggering a change in state for the purpose of locating stuck-at fault bits" (page 15 of amendment). The examiner disagrees, because the independent Claims 1 and 5 only limit the invention to "trigger a change in state of at least one of the memory units". There is no further limitation describing the purpose of the limitation as argued (for the purpose of locating stuck-at fault bits). The examiner reminds the applicant that the features upon which applicant relies (i.e., "for the purpose of locating stuck-at fault bits", and "introducing data into a inaccessible latch in a stuck-at fault LSSD chain") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). And further, the examiner had not used the teachings of the IBM publication for this limitation (underlined above). The Guo reference was used as the teaching for this limitation (see page 5 of Office Action dated 7/27/2004), and so the argument, while not germane to the limitation "for the purpose of locating stuck-at fault bits" as noted above, is also moot because it had failed to address the referenced art. The examiner therefore maintains the rejections of Claims 1-8 under 35 USC 103(a).

Claim Rejections - 35 USC § 112

5. Claim 14 recites the limitation "the stuck-at fault memory unit" in lines 3 and 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. Claims 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over "A Technique for Fault Diagnosis of Defects in Scan Chains", by Guo et al., in view of IBM Technical Disclosure NN81081677.

As per Claim 9:

Guo et al. further teaches the method of Claim 9 including loading all shift register latches of the scan chain with stuck fault output state (see Table 1, SAO and SA1). And in view of the motivation previously stated, the claim is rejected.

As per Claim 10:

Guo et al. teaches a computer readable program for testing combinational and sequential logic circuits where memory (see Abstract) units are coupled together to form shift register latches (see Figure 3) that are arranged in a shift register scan path with an input and output for testing the logic circuits (see Figure 3), the program comprising: stuck fault detection code for detecting a stuck-at fault output level of the shift register scan path from an expect state (page 272, column 2, paragraph 3); shifting data through the scan path to load the shift register latches with the detected stuck-at fault condition (section 4.1 and Table 1); and determining the memory unit furthest from the shift register scan path output that has changed state from its loaded value (page 272 column 1, 2nd paragraph). However, Guo et al. fails to teach causing a permutation of at least one of the following operating parameters: a supply voltage; a reference voltage; a timing pattern temperature and a timing sequence to trigger the said change in state. In the analogous art of NN81081677, such a technique is used

to force a change of state in circuits undergoing "schmoo" testing (second paragraph), where "device power supplies" are varied during testing. The last paragraph states an advantage of reduced test time by alternating test techniques to include voltage and frequency variations. And one with ordinary skill in the art at the time of the invention, motivated as suggested, would find it to be an obvious improvement of Guo et al. by combining the power variation teachings of NN81081677 to speed up an overall test time.

As per Claim 11:

Guo et al. further teaches a computer program of Claim 10 including masking code for masking out all expects for latches following and including a farthest failing latch (page 271, column 2, paragraphs 3 and 4). And in view of the motivation previously stated, the claim is rejected.

As per Claim 12:

NN81081677 further teaches the program of Claim 11, wherein said pattern variation code is for causing permutations in a plurality of the operating parameters (2nd paragraph) centered around a working threshold varying the operating parameters in the vicinity of the working threshold (4th paragraph). And in view of the motivation previously stated, the claim is rejected.

As per Claim 13:

NN81081677 further teaches a computer program of Claim 12 wherein said analyzing code includes shifting code for shifting data out of the scan path after each of the operating parameters is separately permuted (paragraph 6). And in view of the motivation previously stated, the claim is rejected.

As per Claim 14:

Guo et al. further teaches a computer program of Claim 11 wherein said analyzing code includes selection code for selecting the last bit read out that has changed from its load pattern as being from the shift register latch closest to the stuck-at fault memory unit (page 272, column 1, paragraphs 3 and 4). And in view of the motivation previously stated, the claim is rejected.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

Guy J. LAMARRE
PRIMARY EXAMINER